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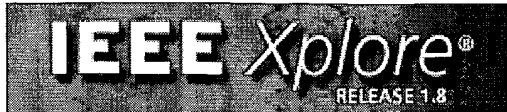
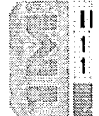
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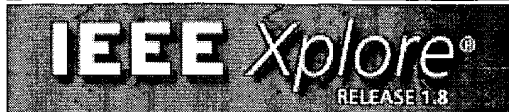
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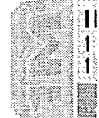
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1 Using negative stuffing retiming for circuit emulation in a packet switching network

Liu, M.-K.;

Communications, IEEE Transactions on , Volume: 40 , Issue: 9 , Sept. 1992
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2 Rate-proportional servers: a design methodology for fair queueing algorithms

Stiliadis, D.; Varma, A.;

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5 Design methodology of a 200 MHz superscalar macroprocessor: SH-Hattori, T.; Nitta, Y.; Seki, M.; Narita, S.; Uchiyama, K.; Takahashi, T.; Satom R.;
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6 A dual-loop delay-locked loop using multiple voltage-controlled delay lines
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7 Digital phased array beamforming using single-bit delta-sigma conversion with non-uniform oversampling
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9 Importance of CAD tools and methodologies in high speed CPU design
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10 Priority inheritance and ceilings for distributed mutual exclusion
Mueller, F.;
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12 Contention resolution with bounded delay

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13 Circuit synthesis of clock distribution networks based on non-zero skew

Neves, J.L.; Friedman, E.G.;

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14 Synthesizing distributed buffer clock trees for high performance AS

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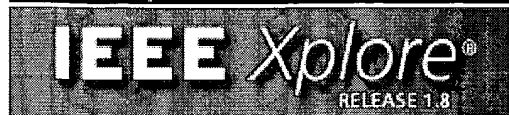
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Zucker, D.F.; Lee, R.B.; Flynn, M.J.;

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Bannatyne, R.;

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4 A 200 MHz 1.2 W 1.4 GFLOPS microprocessor with graphic operation

Nishii, O.; Arakawa, F.; Ishibashi, K.; Nakano, S.; Shimura, T.; Suzuki, K.; Tachibana, M.; Totsuka, Y.; Tsunoda, T.; Uchiyama, K.; Yamada, T.; Hattori, Maejima, H.; Nakagawa, N.; Narita, S.; Seki, M.; Shimazaki, Y.; Satomura, R Takasuga, T.; Hasegawa, A.;

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Treatment codes

P Practical; T Theoretical or Mathematical.

Abstract

Recent developments in transmission and switching technology has made available low-cost gigabit **network** capacity for packet-based WAN (e.g., IP over WDM), that will not require the intermediate SONET/SDH multiplexing layer. For competitive operators that want to minimize their investment by deploying native IP over WDM networks, circuit **emulation** over IP gives support to the important class of legacy circuit-based equipment (e.g., T1/E1 multiplexers), which otherwise will require the deployment of an expensive telecommunication infrastructure, including SONET/SDH equipment. At the user interface, circuit **emulation** is required to maintain the same service of a circuit-based **network**, including synchronization and structured data delivery. In this paper we design the algorithm and the protocol that provide these two features. First, we identify the protocols and mechanisms used in the Internet and their ability to be used for circuit **emulation**. Second, we address the problem of synchronization and we propose an algorithm for efficient source **clock** recovery and handling of **delay** variations. Finally, we show through simulations that circuit **emulation** over IP provides the needed service performance at the user interface. (14 refs).

Descriptors

circuit-switching; packet-switching; protocols; synchronisation;
wavelength-division-multiplexing; wide-area-networks.

Keywords

circuit **emulation**; IP networks; packet based WAN; gigabit **network** capacity; WDM; legacy circuit based equipment; synchronization; structured data delivery; protocol; Internet; source **clock** recovery; **delay** variation; simulations; service performance; user interface.



Classification codes



B6150M (Protocols).
B6210L (Computer communications).
B6150C (Communication switching).
B6260M (Multiplexing and switching in optical communication).
C5640 (Protocols).
C5620W (Other computer networks).

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 locally as:  ☐ include search strategy

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WEST Search History

DATE: Wednesday, September 01, 2004

Hide?	Set Name	Query	Hit Count
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<input type="checkbox"/>	L34	L33 and access cycle	1
<input type="checkbox"/>	L33	L32 and programmable	17
<input type="checkbox"/>	L32	L31 and speed	19
<input type="checkbox"/>	L31	L29 and clock	21
<input type="checkbox"/>	L30	L29 and ready signal	0
<input type="checkbox"/>	L29	emulation near delay\$	27
<input type="checkbox"/>	L28	emulat\$ near delay\$ near ready signal	0
<input type="checkbox"/>	L27	emulat\$ and delay\$ and ready signal	553
<input type="checkbox"/>	L26	L25 and cycle	7
<input type="checkbox"/>	L25	L22 and ready	7
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<input type="checkbox"/>	L21	L20 and speed	11
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<input type="checkbox"/>	L19	L18 and delay\$	25
<input type="checkbox"/>	L18	L17 and network	45
<input type="checkbox"/>	L17	emulation near switch	69
<input type="checkbox"/>	L16	L15 and clock	8
<input type="checkbox"/>	L15	L14 and speed	8
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<input type="checkbox"/>	L13	L11 and emulat\$	4
<input type="checkbox"/>	L12	L11 and L1	0
<input type="checkbox"/>	L11	delay\$ near ready signal	25
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<input type="checkbox"/>	L9	L6 and (emulation near clock)	0
<input type="checkbox"/>	L8	L7 and (emulation near clock)	0
<input type="checkbox"/>	L7	L6 and emulation clock	0
<input type="checkbox"/>	L6	L5 and programmable	57
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<input type="checkbox"/>	L4	L3 and speed	152
<input type="checkbox"/>	L3	L2 and ready signal	154
<input type="checkbox"/>	L2	L1 and cpu	909

☐ L1 emulation and network and clock and delay 1728

END OF SEARCH HISTORY

Hit List

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Generate OACS				

Search Results - Record(s) 1 through 1 of 1 returned.

☒ 1. Document ID: US 20020133325 A1

Using default format because multiple data bases are involved.

L34: Entry 1 of 1

File: PGPB

Sep 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020133325

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020133325 A1

TITLE: Discrete event simulator

PUBLICATION-DATE: September 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Hoare, Raymond R. II	Pittsburgh	PA	US	
Ahn, Jiyong	Pittsburgh	PA	US	
Graves, Jesse	Pittsburgh	PA	US	

US-CL-CURRENT: 703/17

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWMC	Draw D
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Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs	Generate OACS
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Term	Documents
ACCESS	698292
ACCESSES	91204
CYCLE	607778
CYCLES	298482
(33 AND (ACCESS ADJ CYCLE)).PGPB,USPT.	1
(L33 AND ACCESS CYCLE).PGPB,USPT.	1

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[Generate OACS](#)

Search Results - Record(s) 1 through 7 of 7 returned.

☐ 1. Document ID: US 20040085994 A1

Using default format because multiple data bases are involved.

L26: Entry 1 of 7

File: PGPB

May 6, 2004

PGPUB-DOCUMENT-NUMBER: 20040085994

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040085994 A1

TITLE: Methods and apparatus for device access fairness in fibre channel arbitrated loop systems

PUBLICATION-DATE: May 6, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Warren, Bruce Gregory	Poulsbo	WA	US	
Goodwin, William	Bothell	WA	US	
Mies, Carl	Snohomish	WA	US	
Johnson, Bruce E.	Federal Way	WA	US	
White, Michael L.	Oak Harbor	WA	US	
Eng, Warren	Renton	WA	US	

US-CL-CURRENT: 370/462; 370/419

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 2. Document ID: US 20040085974 A1

L26: Entry 2 of 7

File: PGPB

May 6, 2004

PGPUB-DOCUMENT-NUMBER: 20040085974

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040085974 A1

TITLE: Methods and apparatus for device zoning in fibre channel arbitrated loop systems

PUBLICATION-DATE: May 6, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mies, Carl	Snohomish	WA	US	
Warren, Bruce Gregory	Poulsbo	WA	US	

US-CL-CURRENT: 370/406

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 3. Document ID: US 20040085972 A1

L26: Entry 3 of 7

File: PGPB

May 6, 2004

PGPUB-DOCUMENT-NUMBER: 20040085972

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040085972 A1

TITLE: Methods and apparatus for trunking in fibre channel arbitrated loop systems

PUBLICATION-DATE: May 6, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Warren, Bruce Gregory	Poulsbo	WA	US	
Goodwin, William	Bothell	WA	US	
Mies, Carl	Snohomish	WA	US	
Hammond-Doel, Thomas	Everett	WA	US	
White, Michael L.	Oak Harbor	WA	US	

US-CL-CURRENT: 370/401

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 4. Document ID: US 20040081187 A1

L26: Entry 4 of 7

File: PGPB

Apr 29, 2004

PGPUB-DOCUMENT-NUMBER: 20040081187

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040081187 A1

TITLE: Methods and apparatus for switching fibre channel arbitrated loop systems

PUBLICATION-DATE: April 29, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Warren, Bruce Gregory	Poulsbo	WA	US	
Goodman, William P.	Bothell	WA	US	
Mies, Carl	Snohomish	WA	US	
Johnson, Bruce E.	Federal Way	WA	US	
White, Michael L.	Oak Harbor	WA	US	
Eng, Warren	Renton	WA	US	

US-CL-CURRENT: 370/419

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 5. Document ID: US 20040081186 A1

L26: Entry 5 of 7

File: PGPB

Apr 29, 2004

PGPUB-DOCUMENT-NUMBER: 20040081186
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040081186 A1

TITLE: Methods and apparatus for switching Fibre Channel Arbitrated Loop devices

PUBLICATION-DATE: April 29, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Warren, Bruce Gregory	Poulsbo	WA	US	
Goodwin, William	Bothell	WA	US	
Mies, Carl	Snohomish	WA	US	
White, Michael L.	Oak Harbor	WA	US	
Eng, Warren	Renton	WA	US	
Johnson, Bruce E.	Federal Way	WA	US	

US-CL-CURRENT: 370/419

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☒ 6. Document ID: US 6377561 B1

L26: Entry 6 of 7

File: USPT

Apr 23, 2002

US-PAT-NO: 6377561
DOCUMENT-IDENTIFIER: US 6377561 B1

TITLE: Data communication satellite system and method of carrying multi-media traffic

DATE-ISSUED: April 23, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Black; Colin J.	St. Lazare			CA
Takats; Peter	Ile Perrot			CA
Cote; Martin	Montreal			CA
Le-Ngoc; Tho T.	Anjou			CA

US-CL-CURRENT: 370/330

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☒ 7. Document ID: US 4486827 A

L26: Entry 7 of 7

File: USPT

Dec 4, 1984

US-PAT-NO: 4486827

DOCUMENT-IDENTIFIER: US 4486827 A

**** See image for Certificate of Correction ****

TITLE: Microprocessor apparatus

DATE-ISSUED: December 4, 1984

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Shima; Masatoshi	Santa Clara	CA		
Faggin; Federico	Cupertino	CA		
Ungermann; Ralph K.	Los Altos	CA		

US-CL-CURRENT: 710/261

Full	Title	Citation	Front	Review	Classification	Date	Reference	Classification	Classification	Claims	KWIC	Draw. Desc.
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Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs	Generate OACS
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CYCLES	298482
(25 AND CYCLE).PGPB,USPT.	7
(L25 AND CYCLE).PGPB,USPT.	7

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Fwd Refs

Bkwd Refs

Generate OACS

Search Results - Record(s) 1 through 8 of 8 returned.☐ 1. Document ID: US 5426765 A**Using default format because multiple data bases are involved.**

L16: Entry 1 of 8

File: USPT

Jun 20, 1995

US-PAT-NO: 5426765

DOCUMENT-IDENTIFIER: US 5426765 A

TITLE: Multiprocessor cache arbitration

DATE-ISSUED: June 20, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Stevens; Jeffrey C.	Spring	TX		
Jackson; Mike T.	Houston	TX		
Tipley; Roger E.	Houston	TX		
Ramsey; Jens K.	Houston	TX		
Olarig; Sompong	Cypress	TX		
Kelly; Philip C.	Houston	TX		

US-CL-CURRENT: 711/131; 711/146, 711/167

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWC	Draw D
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☐ 2. Document ID: US 5097437 A

L16: Entry 2 of 8

File: USPT

Mar 17, 1992

US-PAT-NO: 5097437

DOCUMENT-IDENTIFIER: US 5097437 A

TITLE: Controller with clocking device controlling first and second state machine controller which generate different control signals for different set of devices

DATE-ISSUED: March 17, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Larson; Ronald J.	Minneapolis	MN	55419	

US-CL-CURRENT: 712/245; 703/25

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWC	Draw D
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☐ 3. Document ID: US 5053947 A

L16: Entry 3 of 8

File: USPT

Oct 1, 1991

US-PAT-NO: 5053947

DOCUMENT-IDENTIFIER: US 5053947 A

TITLE: Extended multistation bus system and method

DATE-ISSUED: October 1, 1991

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Heibel; John T.	Columbus	OH		
Savarda; Raymond R.	Centerburg	OH		

US-CL-CURRENT: 709/237; 370/389, 370/438

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Claims	KWMC	Draw. De
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☐ 4. Document ID: US 4137565 A

L16: Entry 4 of 8

File: USPT

Jan 30, 1979

US-PAT-NO: 4137565

DOCUMENT-IDENTIFIER: US 4137565 A

TITLE: Direct memory access module for a controller

DATE-ISSUED: January 30, 1979

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mager; George E.	Manhattan Beach	CA		
Nelson; Frank M.	Sherman Oaks	CA		
Gillett; Kenneth	Redondo Beach	CA		
Holt; Charles P.	Palos Verdes	CA		
Steiner; Edward L.	Macedon	NY		
Daughton; John W.	Fairport	NY		
Fiske; Kenton W.	Palos Verdes	CA		
Criswell; Thomas	Venice	CA		
Hall; Warren L.	Fairport	NY		

US-CL-CURRENT: 710/22

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Claims	KWMC	Draw. De
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☐ 5. Document ID: US 4131945 A

L16: Entry 5 of 8

File: USPT

Dec 26, 1978

US-PAT-NO: 4131945

DOCUMENT-IDENTIFIER: US 4131945 A

TITLE: Watch dog timer module for a controller

DATE-ISSUED: December 26, 1978

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Richardson; Philip	Pacific Palisades	CA		
Steiner; Edward L.	Macedon	NY		
Daughton; John W.	Fairport	NY		
Fiske; Kenton W.	Fairport	NY		
Criswell; Thomas	Venice	CA		

US-CL-CURRENT: 714/55

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Technical	Claims	KWIC	Drawings
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☐ 6. Document ID: US 4131944 A

L16: Entry 6 of 8

File: USPT

Dec 26, 1978

US-PAT-NO: 4131944

DOCUMENT-IDENTIFIER: US 4131944 A

TITLE: System bus module for a controller

DATE-ISSUED: December 26, 1978

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mager; George E.	Manhattan Beach	CA		
Nelson; Frank M.	Sherman Oaks	CA		
Hall; Warren L.	Palos Verdes	CA		

US-CL-CURRENT: 710/107

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Technical	Claims	KWIC	Drawings
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☐ 7. Document ID: US 4131942 A

L16: Entry 7 of 8

File: USPT

Dec 26, 1978

US-PAT-NO: 4131942

DOCUMENT-IDENTIFIER: US 4131942 A

TITLE: Non-volatile storage module for a controller

DATE-ISSUED: December 26, 1978

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gillett; Kenneth	Redondo Beach	CA		
Steiner; Edward L.	Macedon	NY		
Fiske; Kenton W.	Fairport	NY		
Davis; Kenneth A.	Honeoye Falls	NY		
Kukucka; William P.	Webster	NY		
Criswell; Thomas	Venice	CA		
Richardson; Philip	Pacific Palisades	CA		

US-CL-CURRENT: 714/22

Full	Title	Citation	Front	Review	Classification	Date	Reference	Keywords	Interconnects	Claims	KWIC	Draw D
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☐ 8. Document ID: US 3582628 A

L16: Entry 8 of 8

File: USPT

Jun 1, 1971

US-PAT-NO: 3582628

DOCUMENT-IDENTIFIER: US 3582628 A

TITLE: ANALOG-DIGITAL COMPUTER INTERCONNECTION SYSTEM

DATE-ISSUED: June 1, 1971

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Brussolo; John A.	Ann Arbor	MI		

US-CL-CURRENT: 708/2; 708/6, 708/817, 708/835, 708/840

Full	Title	Citation	Front	Review	Classification	Date	Reference	Keywords	Interconnects	Claims	KWIC	Draw D
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Bkwd Refs

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Term	Documents
CLOCK	272984
CLOCKS	53522
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(L15 AND CLOCK).PGPB,USPT.	8

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Search Results - Record(s) 1 through 4 of 4 returned.

☐ 1. Document ID: US 4137565 A

Using default format because multiple data bases are involved.

L13: Entry 1 of 4

File: USPT

Jan 30, 1979

US-PAT-NO: 4137565

DOCUMENT-IDENTIFIER: US 4137565 A

TITLE: Direct memory access module for a controller

DATE-ISSUED: January 30, 1979

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mager; George E.	Manhattan Beach	CA		
Nelson; Frank M.	Sherman Oaks	CA		
Gillett; Kenneth	Redondo Beach	CA		
Holt; Charles P.	Palos Verdes	CA		
Steiner; Edward L.	Macedon	NY		
Daughton; John W.	Fairport	NY		
Fiske; Kenton W.	Palos Verdes	CA		
Criswell; Thomas	Venice	CA		
Hall; Warren L.	Fairport	NY		

US-CL-CURRENT: 710/22

Full	Title	Citation	Front	Review	Classification	Date	Reference	SEARCHED	INDEXED	Claims	KWIC	Draw. De
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☐ 2. Document ID: US 4131945 A

L13: Entry 2 of 4

File: USPT

Dec 26, 1978

US-PAT-NO: 4131945

DOCUMENT-IDENTIFIER: US 4131945 A

TITLE: Watch dog timer module for a controller

DATE-ISSUED: December 26, 1978

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Richardson; Philip	Pacific Palisades	CA		
Steiner; Edward L.	Macedon	NY		
Daughton; John W.	Fairport	NY		

Fiske; Kenton W. Fairport NY
Criswell; Thomas Venice CA

US-CL-CURRENT: 714/55

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequence	Abstract	Claims	KWMC	Drawings
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☐ 3. Document ID: US 4131944 A

L13: Entry 3 of 4

File: USPT

Dec 26, 1978

US-PAT-NO: 4131944

DOCUMENT-IDENTIFIER: US 4131944 A

TITLE: System bus module for a controller

DATE-ISSUED: December 26, 1978

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mager; George E.	Manhattan Beach	CA		
Nelson; Frank M.	Sherman Oaks	CA		
Hall; Warren L.	Palos Verdes	CA		

US-CL-CURRENT: 710/107

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequence	Abstract	Claims	KWMC	Drawings
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☐ 4. Document ID: US 4131942 A

L13: Entry 4 of 4

File: USPT

Dec 26, 1978

US-PAT-NO: 4131942

DOCUMENT-IDENTIFIER: US 4131942 A

TITLE: Non-volatile storage module for a controller

DATE-ISSUED: December 26, 1978

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gillett; Kenneth	Redondo Beach	CA		
Steiner; Edward L.	Macedon	NY		
Fiske; Kenton W.	Fairport	NY		
Davis; Kenneth A.	Honeoye Falls	NY		
Kukucka; William P.	Webster	NY		
Criswell; Thomas	Venice	CA		
Richardson; Philip	Pacific Palisades	CA		

US-CL-CURRENT: 714/22

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Search Results - Record(s) 1 through 17 of 17 returned.

☒ 1. Document ID: US 20020178427 A1

Using default format because multiple data bases are involved.

L33: Entry 1 of 17

File: PGPB

Nov 28, 2002

PGPUB-DOCUMENT-NUMBER: 20020178427

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020178427 A1

TITLE: Method for improving timing behavior in a hardware logic emulation system

PUBLICATION-DATE: November 28, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ding, Cheng-Liang	Cupertino	CA	US	
Freeman, Thomas H.	Sunnyvale	CA	US	
Chao, Liang-Fang	Cupertino	CA	US	
Ben-Tzur, Tzvi	Sunnyvale	CA	US	

US-CL-CURRENT: 716/12

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWC	Draw. De
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☐ 2. Document ID: US 20020133325 A1

L33: Entry 2 of 17

File: PGPB

Sep 19, 2002

PGPUB-DOCUMENT-NUMBER: 20020133325

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20020133325 A1

TITLE: Discrete event simulator

PUBLICATION-DATE: September 19, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Hoare, Raymond R. II	Pittsburgh	PA	US	
Ahn, Jiyong	Pittsburgh	PA	US	
Graves, Jesse	Pittsburgh	PA	US	

US-CL-CURRENT: 703/17

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWMC	Draw. De
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☒ 3. Document ID: US 20010036188 A1

L33: Entry 3 of 17

File: PGPB

Nov 1, 2001

PGPUB-DOCUMENT-NUMBER: 20010036188

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20010036188 A1

TITLE: Multi-service circuit for telecommunications

PUBLICATION-DATE: November 1, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Carlsson, Dan	Hasselby		SE	

US-CL-CURRENT: 370/395.4; 370/465, 370/535

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWMC	Draw. De
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☐ 4. Document ID: US 6377561 B1

L33: Entry 4 of 17

File: USPT

Apr 23, 2002

US-PAT-NO: 6377561

DOCUMENT-IDENTIFIER: US 6377561 B1

TITLE: Data communication satellite system and method of carrying multi-media traffic

DATE-ISSUED: April 23, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Black; Colin J.	St. Lazare			CA
Takats; Peter	Ile Perrot			CA
Cote; Martin	Montreal			CA
Le-Ngoc; Tho T.	Anjou			CA

US-CL-CURRENT: 370/330

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWMC	Draw. De
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☐ 5. Document ID: US 6256308 B1

L33: Entry 5 of 17

File: USPT

Jul 3, 2001

US-PAT-NO: 6256308

DOCUMENT-IDENTIFIER: US 6256308 B1

TITLE: Multi-service circuit for telecommunications

DATE-ISSUED: July 3, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Carlsson; Dan	Hasselby			SE

US-CL-CURRENT: 370/395.43; 370/395.5, 370/465, 370/535

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequence	Attachments	Claims	KWIC	Drawings
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☐ 6. Document ID: US 5893049 A

L33: Entry 6 of 17

File: USPT

Apr 6, 1999

US-PAT-NO: 5893049

DOCUMENT-IDENTIFIER: US 5893049 A

TITLE: Rapid response voltage threshold determination circuit for electrophysiology diagnostic device

DATE-ISSUED: April 6, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Reggiardo; Christopher V.	Alviso	CA		

US-CL-CURRENT: 702/71; 702/193, 714/735, 714/736

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequence	Attachments	Claims	KWIC	Drawings
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☐ 7. Document ID: US 5835751 A

L33: Entry 7 of 17

File: USPT

Nov 10, 1998

US-PAT-NO: 5835751

DOCUMENT-IDENTIFIER: US 5835751 A

TITLE: Structure and method for providing reconfigurable emulation circuit

DATE-ISSUED: November 10, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chen; Nang-Ping	Cupertino	CA		
Ko; Robert J.	Saratoga	CA		
Li; Jeong-Tyng	Cupertino	CA		
Huang; Thomas B.	San Jose	CA		
Wang; Ming-Yang	Lafayette	CA		

US-CL-CURRENT: 716/16; 327/39

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequence	Abstract	Claims	KWC	Draw D
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☐ 8. Document ID: US 5793356 A

L33: Entry 8 of 17

File: USPT

Aug 11, 1998

US-PAT-NO: 5793356

DOCUMENT-IDENTIFIER: US 5793356 A

TITLE: System and method for the software emulation of a computer joystick

DATE-ISSUED: August 11, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Svancarek; Mark K.	Redmond	WA		
Adan; Manolito E.	Woodinville	WA		
Van Flandern; Michael W.	Redmond	WA		
Pierce; John G.	Vashon	WA		
Suzuki; Hajime	Kanagawa-ken			JP
Kash; Richard B.	Los Altos Hills	CA		

US-CL-CURRENT: 345/161; 345/157, 463/38

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequence	Abstract	Claims	KWC	Draw D
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☐ 9. Document ID: US 5754828 A

L33: Entry 9 of 17

File: USPT

May 19, 1998

US-PAT-NO: 5754828

DOCUMENT-IDENTIFIER: US 5754828 A

**** See image for Certificate of Correction ****

TITLE: System and method for positional control device data source selection

DATE-ISSUED: May 19, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Adan; Manolito E.	Woodinville	WA		
Van Flandern; Michael W.	Redmond	WA		
Dean; Daniel	Issaquah	WA		
Davis; Jeffrey A.	Bothell	WA		

US-CL-CURRENT: 703/24

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequence	Abstract	Claims	KWC	Draw D
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☐ 10. Document ID: US 5724558 A

L33: Entry 10 of 17

File: USPT

Mar 3, 1998

US-PAT-NO: 5724558

DOCUMENT-IDENTIFIER: US 5724558 A

TITLE: System and method for dynamic data packet configuration

DATE-ISSUED: March 3, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Svancarek; Mark K.	Redmond	WA		
Adan; Manolito E.	Woodinville	WA		
Van Flandern; Michael W.	Redmond	WA		
Suzuki; Hajime	Kanagawa-ken			JP

US-CL-CURRENT: 703/21; 345/156, 345/161, 345/168, 703/24, 710/20, 710/58, 712/227, 719/321

Full	Title	Citation	Front	Review	Classification	Date	Reference	Experiments	Attachments	Claims	KWIC	Drawings
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☐ 11. Document ID: US 5716381 A

L33: Entry 11 of 17

File: USPT

Feb 10, 1998

US-PAT-NO: 5716381

DOCUMENT-IDENTIFIER: US 5716381 A

TITLE: Electrophysiology diagnostic device including variable capacitance emulation and voltage threshold determination circuits

DATE-ISSUED: February 10, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Reggiardo; Christopher V.	Alviso	CA		

US-CL-CURRENT: 607/8; 607/5, 607/7

Full	Title	Citation	Front	Review	Classification	Date	Reference	Experiments	Attachments	Claims	KWIC	Drawings
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☐ 12. Document ID: US 5694949 A

L33: Entry 12 of 17

File: USPT

Dec 9, 1997

US-PAT-NO: 5694949

DOCUMENT-IDENTIFIER: US 5694949 A

TITLE: Variable capacitance emulation circuit for electrophysiology diagnostic device

DATE-ISSUED: December 9, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Reggiardo; Christopher V.	Alviso	CA		

US-CL-CURRENT: 128/897; 323/354

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Draw. De
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☐ 13. Document ID: US 5682353 A

L33: Entry 13 of 17

File: USPT

Oct 28, 1997

US-PAT-NO: 5682353

DOCUMENT-IDENTIFIER: US 5682353 A

TITLE: Self adjusting sense amplifier clock delay circuit

DATE-ISSUED: October 28, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Eitan; Boaz	Ra'anana			IL
Petersen; Larry Willis	Pocatello	ID		
Slezak; Yaron	Kiriat Motzkin			IL

US-CL-CURRENT: 365/233; 365/185.21, 365/194, 365/233.5

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Draw. De
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☐ 14. Document ID: US 5649167 A

L33: Entry 14 of 17

File: USPT

Jul 15, 1997

US-PAT-NO: 5649167

DOCUMENT-IDENTIFIER: US 5649167 A

**** See image for Certificate of Correction ****

TITLE: Methods for controlling timing in a logic emulation system

DATE-ISSUED: July 15, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chen; Nang-Ping	Cupertino	CA		
Ko; Robert J.	Saratoga	CA		
Li; Jeong-Tyng	Cupertino	CA		
Huang; Thomas B.	San Jose	CA		
Wang; Ming-Yang	Lafayette	CA		

US-CL-CURRENT: 703/23

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Draw. De
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☐ 15. Document ID: US 5628686 A

L33: Entry 15 of 17

File: USPT

May 13, 1997

US-PAT-NO: 5628686

DOCUMENT-IDENTIFIER: US 5628686 A

TITLE: Apparatus and method for bidirectional data communication in a game port

DATE-ISSUED: May 13, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Svancarek; Mark K.	Redmond	WA		
Adan; Manolito E.	Woodinville	WA		
Van Flandern; Michael W.	Redmond	WA		
Suzuki; Hajime	Kanagawa-ken			JP

US-CL-CURRENT: 463/36

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Claims	KWIC	Draw. De
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☐ 16. Document ID: US 5475830 A

L33: Entry 16 of 17

File: USPT

Dec 12, 1995

US-PAT-NO: 5475830

DOCUMENT-IDENTIFIER: US 5475830 A

TITLE: Structure and method for providing a reconfigurable emulation circuit without hold time violations

DATE-ISSUED: December 12, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chen; Nang-Ping	Cupertino	CA		
Ko; Robert J.	Saratoga	CA		
Li; Jeong-Tyng	Cupertino	CA		
Huang; Thomas B.	San Jose	CA		
Wang; Ming-Yang	Lafayette	CA		

US-CL-CURRENT: 716/16; 716/17, 716/7

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Claims	KWIC	Draw. De
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☐ 17. Document ID: US 5452239 A

L33: Entry 17 of 17

File: USPT

Sep 19, 1995

US-PAT-NO: 5452239

DOCUMENT-IDENTIFIER: US 5452239 A

TITLE: Method of removing gated clocks from the clock nets of a netlist for timing sensitive implementation of the netlist in a hardware emulation system

DATE-ISSUED: September 19, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dai; Wei-Jin	Cupertino	CA		
Galbiati, III; Louis	Mountain View	CA		
Varghese; Joseph	Sunnyvale	CA		
Bui; Dam V.	Milpitas	CA		
Sample; Stephen P.	Mountain View	CA		

US-CL-CURRENT: 703/19; 714/725, 716/17

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Draw D
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Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs	Generate OACS
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Term	Documents
PROGRAMMABLE	168888
PROGRAMMABLES	10
(32 AND PROGRAMMABLE).PGPB,USPT.	17
(L32 AND PROGRAMMABLE).PGPB,USPT.	17

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